UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/410,160	09/30/1999	RISTO BELL	0325.00239	6460

21363 7590 12/23/2004

CHRISTOPHER P. MAIORANA, P.C.
24840 HARPER
ST. CLAIR SHORES, MI 48080

EXAMINER	
GARCIA OTERO, EDUARDO	

ART UNIT	PAPER NUMBER
2123	18

DATE MAILED: 12/23/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

UNITED STATES PATENT AND TRADEMARK OFFICE

Commissioner for Patents
United States Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450
www.uspto.gov

MAILED

DEC 23 2004

Technology Center 2100

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Paper No. 18

Application Number: 09/410,160
Filing Date: September 30, 1999
Appellant(s): BELL ET AL.

Christopher P. Maiorana, Reg. No. 42,829
For Appellant

SUPPLEMENTAL EXAMINER'S ANSWER with NEW GROUNDS OF REJECTION

This is in response to the Remand to the Examiner mailed August 19, 2004 and in response to the memorandum from the Directors of Technical Center 2100 dated September 29, 2004.

The Remand to the Examiner stated "The Office of the Group Director of Technology Center 2100 has requested that this application be remanded". The memorandum from the Directors of Technical Center 2100 (Peggy Fucarino, Stew Levy, and Peter Wong) gave the following instructions to the examiner regarding the remand:

First. The rejection of at least claim 1 is incomplete. The limitation "simulating said design with at least one of said fuses programmed for said repair to verify said repair" is not met by the prior art. Kablanian (U.S. Patent No. 5,764,878) discloses repairing a defective memory cell by severing circuit fuses, therefore at best Kablanian discloses fuses programmed to repair; however, Kablanian makes no mention of simulation as claimed. The examiner's attempt to remedy this defect in the rejection by use of Tzori (U.S. 6,202,044) is improper, as Tzori is not relied upon in the rejection.

Second. The use of the terminology "conventional" does not in and of itself make applicant's statements an admission. The Appellant has made no affirmative statement of admission. Rather, the Appellant has described his own prior practice, which cannot be used against him without evidence that his own prior practice is in fact prior art. See MPEP 2129 regarding "prior art" and "absence of another credible explanation".

Third. For these reasons the rejection of at least claim 1 should be withdrawn. The examiner should find a reference(s), which teaches those elements relied upon as an admission as well as

those elements missing from Kablanian. If no references can be found, it would appear that at least claim 1 is in condition for allowance.

Thus, in view of the memorandum the examiner withdraws the prior rejection of claim 1, and introduces new grounds for rejections below.

(1) Real Party in Interest

A statement identifying the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

A statement identifying the related appeals and interferences which will directly affect or be directly affected by or have a bearing on the decision in the pending appeal is contained in the brief.

(3) Status of Claims

The statement of the status of the claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Invention

The summary of invention contained in the brief is correct.

(6) Issues

New grounds of rejection are provided. Thus the prior issues are moot.

(7) Grouping of Claims

Appellant's brief includes a statement that claims of groups 1-10 do not stand or fall together and provides reasons as set forth in 37 CFR 1.192(c)(7) and (c)(8).

See Brief page 10 for a list of groupings of claims, and see Brief pages 73-75 for detailed reasons.

(8) Claims Appealed

The copy of the appealed claims contained in the Appendix to the brief is correct.

(9) Prior Art of Record

5,841,967	SAMPLE	11-1998
6,202,044	TZORI	3-2001
6,397,349	HIGGINS	5-2002
5,764,878	KABLANIAN	6-1998

Applicant's use of the term "conventional" in the specification is not interpreted as an admission of prior art. See MPEP 2129 regarding "prior art" and "absence of another credible explanation".

(10) Grounds of Rejection (New grounds of rejection are presented)

The following ground(s) of rejection are applicable to the appealed claims:

Claims 1-20 are rejected under 35 USC 103 as unpatentable. New grounds of rejection are presented below. No other rejections are maintained, the 35 USC 112 rejections are withdrawn.

For claim interpretation, please note the following definitions:

Optimization is defined as "[MATH] The maximizing or minimizing of a given function possibly subject to some type of constraints. [SYS ENG] 1. Broadly, the efforts and processes of making a decision, a design, or a system as perfect, **effective, or functional** as possible. 2. Narrowly, the specific methodology, techniques, and procedures used to decide on the one specific solution in a defined set of possible alternatives that will best satisfy a selected criterion. Also known as system optimization." by McGraw–Hill Dictionary of Scientific and Technical Terms, Fourth Edition, page 1329, 1989. Emphasis added.

Simulate is defined as " [ENG] To mimic some or all of the behavior of one system with a different, dissimilar system, particularly with computers, models, or other equipment", according to McGraw-Hill Dictionary of Scientific and Technical Terms, Fourth Edition, page 1737, 1989.

Simulation is defined as "the imitation of the operation of a real-world process or system over time. Simulation involves the generation of an artificial history of the system and the observation of that artificial history to draw inferences concerning the operating characteristics of the real system that is represented. Simulation is an indispensable problem-solving methodology for the solution of many real-world problems. Simulation is used to describe and

analyze the behavior of a system, ask what-if questions about the real system, and aid in the design of real systems. Both existing and conceptual systems can be modeled with simulation." by The Handbook of Simulation, Jerry Banks, 1998, pages 3-4. Note that The Handbook of Simulation specifically addresses modeling existing systems (such as a defective memory) and asking "what-if questions" (such as what-if a given line is repaired).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action: (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

Determining the scope and contents of the prior art.
Ascertaining the differences between the prior art and the claims at issue.
Resolving the level of ordinary skill in the pertinent art.
Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1-20 are rejected under 35 U.S.C. 103(a) as being unpatentable.

Claim 1 (amended) is rejected under 35 U.S.C. 103(a) as being unpatentable over Kablanian and Tzori.

Claim 1 (amended) is an independent claim with 3 limitations.

A-"enumeration of a plurality of fuses" is disclosed by Kablanian Column 2 lines 5-11, "External software is used to determine the optimal utilization of the redundant memory lines to repair defective memory lines. The third process is the repair process. Fuse and/or antifuse equipment facilitates severing circuit fuses that are formed on the chip of selective removal through convention laser beam techniques to repair a defective memory cell".

Kablanian does not explicitly disclose the remaining limitations.

B-"compiling data for each one of said plurality of fuses, wherein said data comprises simulation path data" is disclosed by Tzori at Column 1 line 28 "Performing a Verilog simulation requires that a digital logic designer employ a computer program model for the system by aggregating into a simulation computer program various software modules. The software modules making up a Verilog model include modules for each digital logic circuit included in the simulation, for specifying interconnections among the Verilog logic circuit modules".

C-"simulating said design with at least one of said fuses programmed for said repair to verify said repair" is disclosed by Tzori at Column 1 line 28 "Performing a Verilog simulation requires that a digital logic designer employ a computer program model for the system by aggregating into a simulation computer program various software modules. The software modules making up a Verilog model include modules for each digital logic circuit included in the simulation, for specifying interconnections among the Verilog logic circuit modules".

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to use Tzori to modify Kablalnian. One of ordinary skill in the art would have been motivated to perform analysis using "External software" in order to "determine the optimal utilization" at Kablanian Column 2 line 5.

Note that Kablanian's term "external software" either implicitly discloses, or at least teaches towards using standard commercial simulation software such as the Tzori column 1 line 28 "Verilog simulation". Note that Verilog and VHDL are the most common Hardware Descriptive Languages (HDLs) used in designing integrated circuits. These languages have technical specifications established by IEEE (Institute of Electrical and Electronic Engineers). Specifically, IEEE standard 1364 and IEEE standard 1076 respectively.

Note that Kablanian's term "determine optimum utilization of the redundant memory lines" implies performing simulation of multiple possible solutions and choosing the optimum solution. One of ordinary skill would simulate a circuit design before creating it because that is the standard procedure in the industry in order to save time and money. Simulation is relatively inexpensive in comparison to manufacturing defective circuits.

Additionally, note Tzori Column 1 line 41 states " in almost all instances IC manufacturers simulate their designs before fabricating even a prototype". This same procedure applies to repaired circuits. Note that the repaired circuits of Kablanian are effectively equivalent to prototypes, because the repaired circuits may be unique designs (created by repairing unique failures).

Claim 2 (amended) is rejected under 35 U.S.C. 103(a) as being unpatentable over Kablanian and Tzori.

Claim 2 (amended) depends from Claim 1 (amended) with one additional limitation. Kablanian does not explicitly disclose the additional limitation.

"simulation path data comprises verilog simulation path data" is disclosed by Tzori at Column 1 line 28 "Performing a Verilog simulation requires that a digital logic designer employ a computer program model for the system by aggregating into a simulation computer program various software modules. The software modules making up a Verilog model include modules for each digital logic circuit included in the simulation, for specifying interconnections among the Verilog logic circuit modules".

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to use Tzori to modify Kablalnian. One of ordinary skill in the art would have been motivated to perform analysis using "External software" in order to "determine the optimal utilization" at Kablanian Column 2 line 5.

Note that Kablanian's term "external software" either implicitly discloses, or at least teaches towards using standard commercial simulation software such as the Tzori column 1 line 28 "Verilog simulation". Note that Verilog and VHDL are the most common Hardware Descriptive Languages (HDLs) used in designing integrated circuits. These languages have technical specifications established by IEEE (Institute of Electrical and Electronic Engineers). Note that Kablanian's term "determine optimum utilization of the redundant memory lines" implies performing simulation of multiple possible solutions and choosing the optimum solution. One of ordinary skill would simulate a circuit design before creating it because that is the standard procedure in the industry in order to save time and money. Simulation is relatively inexpensive in comparison to manufacturing defective circuits.

Additionally, note Tzori Column 1 line 41 states " in almost all instances IC manufacturers simulate their designs before fabricating even a prototype". This same procedure applies to repaired circuits. Note that the repaired circuits of Kablanian are similar to prototypes, because the repaired circuits may be unique designs (created by repairing unique failures).

Claim 3 (amended) is rejected under 35 U.S.C. 103(a) as being unpatentable over Kablanian and Tzori and Sample.
Claim 3 (amended) depends from Claim 14 with one additional limitation.
Kablanian does not explicitly disclose the additional limitation.

"said schematic path data comprises schematic paths, properties, hierarchy and a verilog path" is disclosed by Tzori at Column 1 line 28 "Performing a Verilog simulation requires that a digital logic designer employ a computer program model for the system by aggregating into a simulation computer program various software modules. The software modules making up a Verilog model include modules for each digital logic circuit included in the simulation, for specifying interconnections among the Verilog logic circuit modules".

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to use Tzori and Sample to modify Kablalnian. One of ordinary skill in the art would have been motivated to perform analysis using "External software" in order to "determine the optimal utilization" at Kablanian Column 2 line 5.

Note that Kablanian's term "external software" either implicitly discloses, or at least teaches towards using standard commercial simulation software such as the Tzori column 1 line 28 "Verilog simulation". Note that Verilog and VHDL are the most common Hardware Descriptive Languages (HDLs) used in designing integrated circuits. These languages have technical specifications established by IEEE (Institute of Electrical and Electronic Engineers). Note that Kablanian's term "determine optimum utilization of the redundant memory lines" implies performing simulation of multiple possible solutions and choosing the optimum solution. One of ordinary skill would simulate a circuit design before creating it because that is the standard procedure in the industry in order to save time and money. Simulation is relatively inexpensive in comparison to manufacturing defective circuits.

Additionally, note Tzori Column 1 line 41 states " in almost all instances IC manufacturers simulate their designs before fabricating even a prototype". This same procedure applies to repaired circuits. Note that the repaired circuits of Kablanian are similar to prototypes, because the repaired circuits may be unique designs (created by repairing unique failures). Further, note that "the transistor list or layout specification is used to bum [sic] fuses" according to Sample at Column 1 line 46, and burning fuses is precisely what Kablanian is doing.

To summarize, Kablanian implicitly discloses all of the limitations of claim 3. However, Tzori and Sample are used in order to more explicitly disclose the terminology which the applicant uses in the claims.

Claim 4 (twice amended) is rejected under 35 U.S.C. 103(a) as being unpatentable over Kablanian and Tzori and Sample.
Claim 4 (twice amended) depends from Claim 1 (amended) with one additional limitation. Kablanian does not explicitly disclose the additional limitation.

"step (B) further comprises the sub-step of: generating a list of layout coordinates and paths as part of said compiling" is disclosed by Sample at FIG 13 element 140 "NETLIST GENERATOR" and element 148 "PART, PLACE, ROUTE", and Sample Column 1 line 46 "the transistor list or layout specification is used to bum [sic] fuses".

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to use Tzori and Sample to modify Kablalnian. One of ordinary skill in the art would have been motivated to perform analysis using "External software" in order to "determine the optimal utilization" at Kablanian Column 2 line 5.

Note that Kablanian's term "external software" either implicitly discloses, or at least teaches towards using standard commercial simulation software such as the Tzori column 1 line 28 "Verilog simulation". Note that Verilog and VHDL are the most common Hardware Descriptive Languages (HDLs) used in designing integrated circuits. These languages have technical specifications established by IEEE (Institute of Electrical and Electronic Engineers). Note that Kablanian's term "determine optimum utilization of the redundant memory lines" implies performing simulation of multiple possible solutions and choosing the optimum solution. One of ordinary skill would simulate a circuit design before creating it because that is the

standard procedure in the industry in order to save time and money. Simulation is relatively inexpensive in comparison to manufacturing defective circuits.

Additionally, note Tzori Column 1 line 41 states " in almost all instances IC manufacturers simulate their designs before fabricating even a prototype". This same procedure applies to repaired circuits. Note that the repaired circuits of Kablanian are similar to prototypes, because the repaired circuits may be unique designs (created by repairing unique failures).

Further, note that "the transistor list or layout specification is used to bum [sic] fuses" according to Sample at Column 1 line 46, and burning fuses is precisely what Kablanian is doing.

Claim 5 (amended) is rejected under 35 U.S.C. 103(a) as being unpatentable over Kablanian and Tzori and Sample

Claim 5 (amended) depends from Claim 1 (amended) with one additional limitation.

"generating a fuse report" is disclosed by Sample at FIG 13 element 140 "NETLIST GENERATOR" and element 148 "PART, PLACE, ROUTE", and Sample Column 1 line 46 "the transistor list or layout specification is used to bum [sic] fuses".

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to use Tzori and Sample to modify Kablalnian. One of ordinary skill in the art would have been motivated to perform analysis using "External software" in order to "determine the optimal utilization" at Kablanian Column 2 line 5.

Note that Kablanian's term "external software" either implicitly discloses, or at least teaches towards using standard commercial simulation software such as the Tzori column 1 line 28 "Verilog simulation". Note that Verilog and VHDL are the most common Hardware Descriptive Languages (HDLs) used in designing integrated circuits. These languages have technical specifications established by IEEE (Institute of Electrical and Electronic Engineers). Note that Kablanian's term "determine optimum utilization of the redundant memory lines" implies performing simulation of multiple possible solutions and choosing the optimum solution. One of ordinary skill would simulate a circuit design before creating it because that is the standard procedure in the industry in order to save time and money. Simulation is relatively inexpensive in comparison to manufacturing defective circuits.

Additionally, note Tzori Column 1 line 41 states " in almost all instances IC manufacturers simulate their designs before fabricating even a prototype". This same procedure applies to repaired circuits. Note that the repaired circuits of Kablanian are similar to prototypes, because the repaired circuits may be unique designs (created by repairing unique failures).

Further, note that "the transistor list or layout specification is used to bum [sic] fuses" according to Sample at Column 1 line 46, and burning fuses is precisely what Kablanian is doing.

Claim 6 (amended) is rejected under 35 U.S.C. 103(a) as being unpatentable over Kablanian and Tzori and Sample.

Claim 6 (amended) depends from Claim 5 (amended) with one additional limitation. Kablanian does not explicitly disclose the additional limitation.

"listing physical location of one or more devices in response to said fuse reports" is Sample at FIG 13 element 140 "NETLIST GENERATOR" and element 148 "PART, PLACE, ROUTE", and Sample Column 1 line 46 "the transistor list or layout specification is used to bum [sic] fuses".

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to use Tzori and Sample to modify Kablalnian. One of ordinary skill in the art would have been motivated to perform analysis using "External software" in order to "determine the optimal utilization" at Kablanian Column 2 line 5.

Note that Kablanian's term "external software" either implicitly discloses, or at least teaches towards using standard commercial simulation software such as the Tzori column 1 line 28 "Verilog simulation". Note that Verilog and VHDL are the most common Hardware Descriptive Languages (HDLs) used in designing integrated circuits. These languages have technical specifications established by IEEE (Institute of Electrical and Electronic Engineers). Note that Kablanian's term "determine optimum utilization of the redundant memory lines" implies performing simulation of multiple possible solutions and choosing the optimum solution. One of ordinary skill would simulate a circuit design before creating it because that is the standard procedure in the industry in order to save time and money. Simulation is relatively inexpensive in comparison to manufacturing defective circuits.

Additionally, note Tzori Column 1 line 41 states " in almost all instances IC manufacturers simulate their designs before fabricating even a prototype". This same procedure applies to repaired circuits. Note that the repaired circuits of Kablanian are similar to prototypes, because the repaired circuits may be unique designs (created by repairing unique failures).

Further, note that "the transistor list or layout specification is used to bum [sic] fuses" according to Sample at Column 1 line 46, and burning fuses is precisely what Kablanian is doing.

Claim 7 (amended) is rejected under 35 U.S.C. 103(a) as being unpatentable over Kablanian and Tzori and Sample.
Claim 7 (amended) depends from Claim 1 (amended) with one new limitation.
Kablanian does not explicitly disclose the additional limitation.

"generating a repair file that predicts said at least one of said fuses programmed for said repair" is disclosed by Sample at FIG 13 element 140 "NETLIST GENERATOR" and element 148 "PART, PLACE, ROUTE", and Sample Column 1 line 46 "the transistor list or layout specification is used to bum [sic] fuses".

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to use Tzori and Sample to modify Kablalnian. One of ordinary skill in the art would have been motivated to perform analysis using "External software" in order to "determine the optimal utilization" at Kablanian Column 2 line 5.

Note that Kablanian's term "external software" either implicitly discloses, or at least teaches towards using standard commercial simulation software such as the Tzori column 1 line 28 "Verilog simulation". Note that Verilog and VHDL are the most common Hardware Descriptive Languages (HDLs) used in designing integrated circuits. These languages have technical specifications established by IEEE (Institute of Electrical and Electronic Engineers). Note that Kablanian's term "determine optimum utilization of the redundant memory lines" implies performing simulation of multiple possible solutions and choosing the optimum solution. One of ordinary skill would simulate a circuit design before creating it because that is the standard procedure in the industry in order to save time and money. Simulation is relatively inexpensive in comparison to manufacturing defective circuits.

Additionally, note Tzori Column 1 line 41 states " in almost all instances IC manufacturers simulate their designs before fabricating even a prototype". This same procedure applies to repaired circuits. Note that the repaired circuits of Kablanian are similar to prototypes, because the repaired circuits may be unique designs (created by repairing unique failures).

Further, note that "the transistor list or layout specification is used to bum [sic] fuses" according to Sample at Column 1 line 46, and burning fuses is precisely what Kablanian is doing.

Claim 8 (amended) is rejected under 35 U.S.C. 103(a) as being unpatentable over Kablanian and Tzori and Sample and Higgins.
Claim 8 (amended) depends from Claim 7 (amended) with one additional limitation.
Kablanian does not explicitly disclose the additional limitation.

"creating a repair program in response to said repair file" is disclosed by Higgins Column 1 line 20 "Location information is then supplied to a controller for a laser repair device, which achieves a hardware fix."

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to use Tzori and Sample and Higgins to modify Kablalnian. One of ordinary skill in the art would have been motivated to perform analysis using "External software" in order to "determine the optimal utilization" at Kablanian Column 2 line 5.

Note that Kablanian's term "external software" either implicitly discloses, or at least teaches towards using standard commercial simulation software such as the Tzori column 1 line 28 "Verilog simulation". Note that Verilog and VHDL are the most common Hardware Descriptive Languages (HDLs) used in designing integrated circuits. These languages have technical specifications established by IEEE (Institute of Electrical and Electronic Engineers). Note that Kablanian's term "determine optimum utilization of the redundant memory lines" implies performing simulation of multiple possible solutions and choosing the optimum solution. One of ordinary skill would simulate a circuit design before creating it because that is the standard procedure in the industry in order to save time and money. Simulation is relatively inexpensive in comparison to manufacturing defective circuits. Note Higgins column 1 line 24 states "repair procedures result in higher yields".

Additionally, note Tzori Column 1 line 41 states " in almost all instances IC manufacturers simulate their designs before fabricating even a prototype". This same procedure applies to repaired circuits. Note that the repaired circuits of Kablanian are similar to prototypes, because the repaired circuits may be unique designs (created by repairing unique failures). Further, note that "the transistor list or layout specification is used to bum [sic] fuses" according to Sample at Column 1 line 46, and burning fuses is precisely what Kablanian is doing.

To summarize, Kablanian implicitly discloses all of the limitations of claim 8. However, Tzori and Sample and Higgins are used in order to more explicitly disclose the terminology which the applicant uses in the claims.

Claim 9 (amended) is rejected under 35 U.S.C. 103(a) as being unpatentable over Kablanian and Tzori and Sample and Higgins.
Claim 9 (amended) depends from Claim 8 (amended) with one additional limitation.
Kablanian does not explicitly disclose the additional limitation.

"verifying a function of said design in response to said repair program" is disclosed by Tzori at Column 1 line 17 "Various different software and hardware systems exist for simulating and/or emulating".

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to use Tzori and Sample and Higgins to modify Kablalnian. One of ordinary skill in the art would have been motivated to perform analysis using "External software" in order to "determine the optimal utilization" at Kablanian Column 2 line 5.

Note that Kablanian's term "external software" either implicitly discloses, or at least teaches towards using standard commercial simulation software such as the Tzori column 1 line 28 "Verilog simulation". Note that Verilog and VHDL are the most common Hardware Descriptive Languages (HDLs) used in designing integrated circuits. These languages have technical specifications established by IEEE (Institute of Electrical and Electronic Engineers). Note that Kablanian's term "determine optimum utilization of the redundant memory lines" implies performing simulation of multiple possible solutions and choosing the optimum solution. One of ordinary skill would simulate a circuit design before creating it because that is the standard procedure in the industry in order to save time and money. Simulation is relatively

inexpensive in comparison to manufacturing defective circuits. Note Higgins column 1 line 24 states "repair procedures result in higher yields".

Additionally, note Tzori Column 1 line 41 states " in almost all instances IC manufacturers simulate their designs before fabricating even a prototype". This same procedure applies to repaired circuits. Note that the repaired circuits of Kablanian are similar to prototypes, because the repaired circuits may be unique designs (created by repairing unique failures). Further, note that "the transistor list or layout specification is used to bum [sic] fuses" according to Sample at Column 1 line 46, and burning fuses is precisely what Kablanian is doing.

To summarize, Kablanian implicitly discloses all of the limitations of claim 9. However, Tzori and Sample and Higgins are used in order to more explicitly disclose the terminology which the applicant uses in the claims.

Claim 10 (amended) is rejected under 35 U.S.C. 103(a) as being unpatentable over Kablanian and Tzori and Sample and Higgins.
Claim 10 (amended) depends from Claim 8 (amended) with one additional limitation. Kablanian does not explicitly disclose the additional limitation.

"listing an output of said repair program as a list of coordinates for said at least one of said fuses programmed for said repair in terms of a plurality of logical addresses" is disclosed by Sample at FIG 13 element 140 "NETLIST GENERATOR" and element 148 "PART, PLACE, ROUTE", and Sample Column 1 line 46 "the transistor list or layout specification is used to bum [sic] fuses".

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to use Tzori and Sample and Higgins to modify Kablalnian. One of ordinary skill in the art would have been motivated to perform analysis using "External software" in order to "determine the optimal utilization" at Kablanian Column 2 line 5.

Note that Kablanian's term "external software" either implicitly discloses, or at least teaches towards using standard commercial simulation software such as the Tzori column 1 line 28 "Verilog simulation". Note that Verilog and VHDL are the most common Hardware Descriptive Languages (HDLs) used in designing integrated circuits. These languages have technical specifications established by IEEE (Institute of Electrical and Electronic Engineers).

Note that Kablanian's term "determine optimum utilization of the redundant memory lines" implies performing simulation of multiple possible solutions and choosing the optimum solution. One of ordinary skill would simulate a circuit design before creating it because that is the standard procedure in the industry in order to save time and money. Simulation is relatively inexpensive in comparison to manufacturing defective circuits. Note Higgins column 1 line 24 states "repair procedures result in higher yields".

Additionally, note Tzori Column 1 line 41 states " in almost all instances IC manufacturers simulate their designs before fabricating even a prototype". This same procedure applies to repaired circuits. Note that the repaired circuits of Kablanian are similar to prototypes, because the repaired circuits may be unique designs (created by repairing unique failures). Further, note that "the transistor list or layout specification is used to bum [sic] fuses" according to Sample at Column 1 line 46, and burning fuses is precisely what Kablanian is doing.

To summarize, Kablanian implicitly discloses all of the limitations of claim 10. However, Tzori and Sample and Higgins are used in order to more explicitly disclose the terminology which the applicant uses in the claims.

Claim 11 (amended) is rejected under 35 U.S.C. 103(a) as being unpatentable over Kablanian and Tzori and Sample and Higgins.
Claim 11 (amended) depends from Claim 10 (amended) with one new limitation.
Kablanian does not explicitly disclose the additional limitation.

"storing said coordinates in a memory" is disclosed by Sample at FIG 13 element 140 "NETLIST GENERATOR" and element 148 "PART, PLACE, ROUTE", and Sample Column 1 line 46 "the transistor list or layout specification is used to bum [sic] fuses". Note that said transistor list and routes are inherently stored in memory during software simulation.

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to use Tzori and Sample and Higgins to modify Kablalnian. One of ordinary skill in the art would have been motivated to perform analysis using "External software" in order to "determine the optimal utilization" at Kablanian Column 2 line 5.

Note that Kablanian's term "external software" either implicitly discloses, or at least teaches towards using standard commercial simulation software such as the Tzori column 1 line

28 "Verilog simulation". Note that Verilog and VHDL are the most common Hardware Descriptive Languages (HDLs) used in designing integrated circuits. These languages have technical specifications established by IEEE (Institute of Electrical and Electronic Engineers). Note that Kablanian's term "determine optimum utilization of the redundant memory lines" implies performing simulation of multiple possible solutions and choosing the optimum solution. One of ordinary skill would simulate a circuit design before creating it because that is the standard procedure in the industry in order to save time and money. Simulation is relatively inexpensive in comparison to manufacturing defective circuits. Note Higgins column 1 line 24 states "repair procedures result in higher yields".

Additionally, note Tzori Column 1 line 41 states " in almost all instances IC manufacturers simulate their designs before fabricating even a prototype". This same procedure applies to repaired circuits. Note that the repaired circuits of Kablanian are similar to prototypes, because the repaired circuits may be unique designs (created by repairing unique failures).

Further, note that "the transistor list or layout specification is used to bum [sic] fuses" according to Sample at Column 1 line 46, and burning fuses is precisely what Kablanian is doing.

To summarize, Kablanian implicitly discloses all of the limitations of claim 11. However, Tzori and Sample and Higgins are used in order to more explicitly disclose the terminology which the applicant uses in the claims.

Claim 12 (amended) is rejected under 35 U.S.C. 103(a).

Claim 12 (amended) is an independent "apparatus" claim with the same limitations as Claim 1, and thus is rejected for the same reasons.

Claim 13 (amended) is rejected under 35 U.S.C. 103(a).

Claim 13 (amended) is an "apparatus" claim with "means for" language and with the same limitations as Claim 1, and thus is rejected for the same reasons.

Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kablanian and Tzori and Sample.

Claim 14 depends from Claim 1, with one additional limitation.
Kablanian does not explicitly disclose the additional limitation.

"said data further comprises schematic path data" is disclosed by Sample at FIG 13 element 140 "NETLIST GENERATOR" and element 148 "PART, PLACE, ROUTE", and Sample Column 1 line 46 "the transistor list or layout specification is used to bum [sic] fuses".

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to use Tzori and Sample to modify Kablalnian. One of ordinary skill in the art would have been motivated to perform analysis using "External software" in order to "determine the optimal utilization" at Kablanian Column 2 line 5.

Note that Kablanian's term "external software" either implicitly discloses, or at least teaches towards using standard commercial simulation software such as the Tzori column 1 line 28 "Verilog simulation". Note that Verilog and VHDL are the most common Hardware Descriptive Languages (HDLs) used in designing integrated circuits. These languages have technical specifications established by IEEE (Institute of Electrical and Electronic Engineers). Note that Kablanian's term "determine optimum utilization of the redundant memory lines" implies performing simulation of multiple possible solutions and choosing the optimum solution. One of ordinary skill would simulate a circuit design before creating it because that is the standard procedure in the industry in order to save time and money. Simulation is relatively inexpensive in comparison to manufacturing defective circuits.

Additionally, note Tzori Column 1 line 41 states " in almost all instances IC manufacturers simulate their designs before fabricating even a prototype". This same procedure applies to repaired circuits. Note that the repaired circuits of Kablanian are similar to prototypes, because the repaired circuits may be unique designs (created by repairing unique failures).

Further, note that "the transistor list or layout specification is used to bum [sic] fuses" according to Sample at Column 1 line 46, and burning fuses is precisely what Kablanian is doing.

To summarize, Kablanian implicitly discloses all of the limitations of claim 14. However, Tzori and Sample are used in order to more explicitly disclose the terminology which the applicant uses in the claims.

Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kablanian and Tzori and Sample.

Claim 15 depends from Claim 1, with one additional limitation.

Kablanian does not explicitly disclose the additional limitation.

"said data further comprises physical layout data" is disclosed by Sample at FIG 13 element 140 "NETLIST GENERATOR" and element 148 "PART, PLACE, ROUTE", and Sample Column 1 line 46 "the transistor list or layout specification is used to bum [sic] fuses".

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to use Tzori and Sample to modify Kablalnian. One of ordinary skill in the art would have been motivated to perform analysis using "External software" in order to "determine the optimal utilization" at Kablanian Column 2 line 5.

Note that Kablanian's term "external software" either implicitly discloses, or at least teaches towards using standard commercial simulation software such as the Tzori column 1 line 28 "Verilog simulation". Note that Verilog and VHDL are the most common Hardware Descriptive Languages (HDLs) used in designing integrated circuits. These languages have technical specifications established by IEEE (Institute of Electrical and Electronic Engineers). Note that Kablanian's term "determine optimum utilization of the redundant memory lines" implies performing simulation of multiple possible solutions and choosing the optimum solution. One of ordinary skill would simulate a circuit design before creating it because that is the standard procedure in the industry in order to save time and money. Simulation is relatively inexpensive in comparison to manufacturing defective circuits.

Additionally, note Tzori Column 1 line 41 states " in almost all instances IC manufacturers simulate their designs before fabricating even a prototype". This same procedure applies to repaired circuits. Note that the repaired circuits of Kablanian are similar to prototypes, because the repaired circuits may be unique designs (created by repairing unique failures). Further, note that "the transistor list or layout specification is used to bum [sic] fuses" according to Sample at Column 1 line 46, and burning fuses is precisely what Kablanian is doing.

To summarize, Kablanian implicitly discloses all of the limitations of claim 15. However, Tzori and Sample are used in order to more explicitly disclose the terminology which the applicant uses in the claims.

Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kablanian and Tzori and Sample.

Claim 16 depends from Claim 1, with one additional limitation.

Kablanian does not explicitly disclose the additional limitation.

"mapping a plurality of co-ordinates of said fuses to a plurality of verilog statements" is disclosed by Sample at FIG 13 element 140 "NETLIST GENERATOR" and element 148 "PART, PLACE, ROUTE", and Sample Column 1 line 46 "the transistor list or layout specification is used to bum [sic] fuses".

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to use Tzori and Sample to modify Kablalnian. One of ordinary skill in the art would have been motivated to perform analysis using "External software" in order to "determine the optimal utilization" at Kablanian Column 2 line 5.

Note that Kablanian's term "external software" either implicitly discloses, or at least teaches towards using standard commercial simulation software such as the Tzori column 1 line 28 "Verilog simulation". Note that Verilog and VHDL are the most common Hardware Descriptive Languages (HDLs) used in designing integrated circuits. These languages have technical specifications established by IEEE (Institute of Electrical and Electronic Engineers). Note that Kablanian's term "determine optimum utilization of the redundant memory lines" implies performing simulation of multiple possible solutions and choosing the optimum solution. One of ordinary skill would simulate a circuit design before creating it because that is the standard procedure in the industry in order to save time and money. Simulation is relatively inexpensive in comparison to manufacturing defective circuits.

Additionally, note Tzori Column 1 line 41 states " in almost all instances IC manufacturers simulate their designs before fabricating even a prototype". This same procedure applies to repaired circuits. Note that the repaired circuits of Kablanian are similar to prototypes, because the repaired circuits may be unique designs (created by repairing unique failures). Further, note that "the transistor list or layout specification is used to bum [sic] fuses" according to Sample at Column 1 line 46, and burning fuses is precisely what Kablanian is doing.

To summarize, Kablanian implicitly discloses all of the limitations of claim 16. However, Tzori and Sample are used in order to more explicitly disclose the terminology which the applicant uses in the claims.

Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kablanian and Tzori and Sample and Higgins.

Claim 17 depends from Claim 8, with one additional limitation.

Kablanian does not explicitly disclose the additional limitation.

"checking said repair file and said repair program for an error" is disclosed by is disclosed by Tzori at Column 1 line 17 "Various different software and hardware systems exist for simulating and/or emulating".

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to use Tzori and Sample and Higgins to modify Kablalnian. One of ordinary skill in the art would have been motivated to perform analysis using "External software" in order to "determine the optimal utilization" at Kablanian Column 2 line 5.

Note that Kablanian's term "external software" either implicitly discloses, or at least teaches towards using standard commercial simulation software such as the Tzori column 1 line 28 "Verilog simulation". Note that Verilog and VHDL are the most common Hardware Descriptive Languages (HDLs) used in designing integrated circuits. These languages have technical specifications established by IEEE (Institute of Electrical and Electronic Engineers). Note that Kablanian's term "determine optimum utilization of the redundant memory lines" implies performing simulation of multiple possible solutions and choosing the optimum solution. One of ordinary skill would simulate a circuit design before creating it because that is the standard procedure in the industry in order to save time and money. Simulation is relatively inexpensive in comparison to manufacturing defective circuits.

Additionally, note Tzori Column 1 line 41 states " in almost all instances IC manufacturers simulate their designs before fabricating even a prototype". This same procedure applies to repaired circuits. Note that the repaired circuits of Kablanian are similar to prototypes, because the repaired circuits may be unique designs (created by repairing unique failures).

Further, note that "the transistor list or layout specification is used to bum [sic] fuses" according to Sample at Column 1 line 46, and burning fuses is precisely what Kablanian is doing.

To summarize, Kablanian implicitly discloses all of the limitations of claim 17. However, Tzori and Sample and Higgins are used in order to more explicitly disclose the terminology which the applicant uses in the claims.

Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kablanian and Tzori.

Claim 18 depends from Claim 12, with one additional limitation.

Kablanian does not explicitly disclose the additional limitation.

"said first circuit is further configured to provide an elevation of said fuses at least one level of abstraction in said design" is disclosed by Tzori at Column 1 line 28 "Performing a Verilog simulation requires that a digital logic designer employ a computer program model for the system by aggregating into a simulation computer program various software modules. The software modules making up a Verilog model include modules for each digital logic circuit included in the simulation, for specifying interconnections among the Verilog logic circuit modules".

Note that Verilog inherently contains at least one level of abstraction. Specifically, Verilog defines the circuit using at least one of four possible levels of abstraction: gate, logic, RTL, or algorithm.

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to use Tzori modify Kablalnian. One of ordinary skill in the art would have been motivated to perform analysis using "External software" in order to "determine the optimal utilization" at Kablanian Column 2 line 5.

Note that Kablanian's term "external software" either implicitly discloses, or at least teaches towards using standard commercial simulation software such as the Tzori column 1 line 28 "Verilog simulation". Note that Verilog and VHDL are the most common Hardware Descriptive Languages (HDLs) used in designing integrated circuits. These languages have technical specifications established by IEEE (Institute of Electrical and Electronic Engineers). Note that Kablanian's term "determine optimum utilization of the redundant memory lines"

implies performing simulation of multiple possible solutions and choosing the optimum solution. One of ordinary skill would simulate a circuit design before creating it because that is the standard procedure in the industry in order to save time and money. Simulation is relatively inexpensive in comparison to manufacturing defective circuits.

Additionally, note Tzori Column 1 line 41 states " in almost all instances IC manufacturers simulate their designs before fabricating even a prototype". This same procedure applies to repaired circuits. Note that the repaired circuits of Kablanian are similar to prototypes, because the repaired circuits may be unique designs (created by repairing unique failures). Further, note that "the transistor list or layout specification is used to bum [sic] fuses" according to Sample at Column 1 line 46, and burning fuses is precisely what Kablanian is doing.

To summarize, Kablanian implicitly discloses all of the limitations of claim 18. However, Tzori is used in order to more explicitly disclose the terminology which the applicant uses in the claims.

Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kablanian and Tzori.

Claim 19 depends from Claim 12, with one additional limitation.

Kablanian does not explicitly disclose the additional limitation.

"said first circuit is further configured to collect data relevant to said fuses that are grouped" is disclosed by Tzori at Column 1 line 28 "Performing a Verilog simulation requires that a digital logic designer employ a computer program model for the system by aggregating into a simulation computer program various software modules. The software modules making up a Verilog model include modules for each digital logic circuit included in the simulation, for specifying interconnections among the Verilog logic circuit modules". Note that Verilog inherently contains at least one level of abstraction.

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to use Tzori modify Kablalnian. One of ordinary skill in the art would have been motivated to perform analysis using "External software" in order to "determine the optimal utilization" at Kablanian Column 2 line 5.

Note that Kablanian's term "external software" either implicitly discloses, or at least teaches towards using standard commercial simulation software such as the Tzori column 1 line 28 "Verilog simulation". Note that Verilog and VHDL are the most common Hardware Descriptive Languages (HDLs) used in designing integrated circuits. These languages have technical specifications established by IEEE (Institute of Electrical and Electronic Engineers). Note that Kablanian's term "determine optimum utilization of the redundant memory lines" implies performing simulation of multiple possible solutions and choosing the optimum solution. One of ordinary skill would simulate a circuit design before creating it because that is the standard procedure in the industry in order to save time and money. Simulation is relatively inexpensive in comparison to manufacturing defective circuits.

Additionally, note Tzori Column 1 line 41 states " in almost all instances IC manufacturers simulate their designs before fabricating even a prototype". This same procedure applies to repaired circuits. Note that the repaired circuits of Kablanian are similar to prototypes, because the repaired circuits may be unique designs (created by repairing unique failures). Further, note that "the transistor list or layout specification is used to bum [sic] fuses" according to Sample at Column 1 line 46, and burning fuses is precisely what Kablanian is doing.

To summarize, Kablanian implicitly discloses all of the limitations of claim 19. However, Tzori is used in order to more explicitly disclose the terminology which the applicant uses in the claims.

Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kablanian and Tzori and Sample.

Claim 20 depends from Claim 12, with one additional limitation.

"said second circuit is further configured to write a report file" is disclosed by Sample at FIG 13 element 140 "NETLIST GENERATOR" and element 148 "PART, PLACE, ROUTE", and Sample Column 1 line 46 "the transistor list or layout specification is used to bum [sic] fuses".

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to use Tzori and Sample to modify Kablalnian. One of ordinary skill in the art

would have been motivated to perform analysis using "External software" in order to "determine the optimal utilization" at Kablanian Column 2 line 5.

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to use Tzori and Sample modify Kablalnian. One of ordinary skill in the art would have been motivated to perform analysis using "External software" in order to "determine the optimal utilization" at Kablanian Column 2 line 5.

Note that Kablanian's term "external software" either implicitly discloses, or at least teaches towards using standard commercial simulation software such as the Tzori column 1 line 28 "Verilog simulation". Note that Verilog and VHDL are the most common Hardware Descriptive Languages (HDLs) used in designing integrated circuits. These languages have technical specifications established by IEEE (Institute of Electrical and Electronic Engineers). Note that Kablanian's term "determine optimum utilization of the redundant memory lines" implies performing simulation of multiple possible solutions and choosing the optimum solution. One of ordinary skill would simulate a circuit design before creating it because that is the standard procedure in the industry in order to save time and money. Simulation is relatively inexpensive in comparison to manufacturing defective circuits.

Additionally, note Tzori Column 1 line 41 states " in almost all instances IC manufacturers simulate their designs before fabricating even a prototype". This same procedure applies to repaired circuits. Note that the repaired circuits of Kablanian are similar to prototypes, because the repaired circuits may be unique designs (created by repairing unique failures). Further, note that "the transistor list or layout specification is used to bum [sic] fuses" according to Sample at Column 1 line 46, and burning fuses is precisely what Kablanian is doing.

To summarize, Kablanian implicitly discloses all of the limitations of claim 19. However, Tzori and Sample are used in order to more explicitly disclose the terminology which the applicant uses in the claims.

(11) Response to Argument

Applicant's argument that the specification term "conventional" is not admission of prior art is persuasive.

Applicant's argument that all the limitations of claim 1 are not expressly disclosed by the cited prior art is persuasive.

In view of Applicant's persuasive arguments, new grounds for rejection are presented below. Note that no new prior art is presented.

All claims are rejected under 35 USC 103 using new grounds of rejection.

(11.11) GROUPS 1-10 ARE SEPARATELY PATENTABLE. Brief pages 73-75.

Applicant gives detailed reasons why each of Groups 1-10 are separately patentable. The Examiner agrees with these reasons.

(11.12) SUMMARY.

All pending 35 USC 112 rejections are withdrawn (claims 1 and 7).

New grounds of rejection under 35 USC 103 rejections are provided for all claims (claims 1-20).

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Eduardo Garcia-Otero Eduardo Garcia Otero 10/8/04

Conferees:
William Thomson
Kevin Teska, Supervisor, Art Unit 2123

KEVIN J. TESKA
SUPERVISORY
PATENT EXAMINER

CHRISTOPHER P. MAIORANA, P.C.
24025 GREATER MACK
SUITE 200
ST. CLAIR SHORES, MI 48080